BMEN 428/ECEN 489
CSCE 489/BMEN 689

Laboratory Presentations

Clocks and Low Power Modes

Please **SIGN IN** at the front!

Turn in all **POST LABS** at the front!

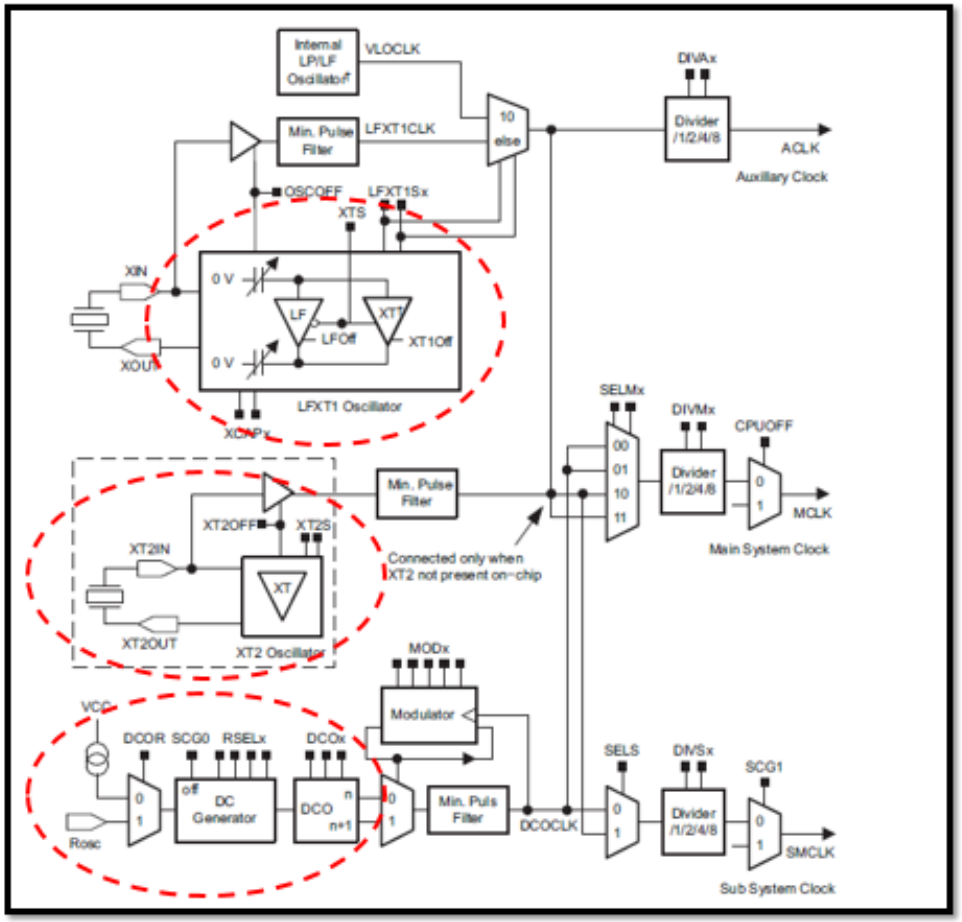
Basic Clock Module+

Oscillator Sources

– **LFXT1CLK**: Low-frequency/high-frequency oscillator

– **T2CLK**: Optional high-frequency oscillator

– **DCOCLK**: Internal digitally controlled oscillator (DCO)



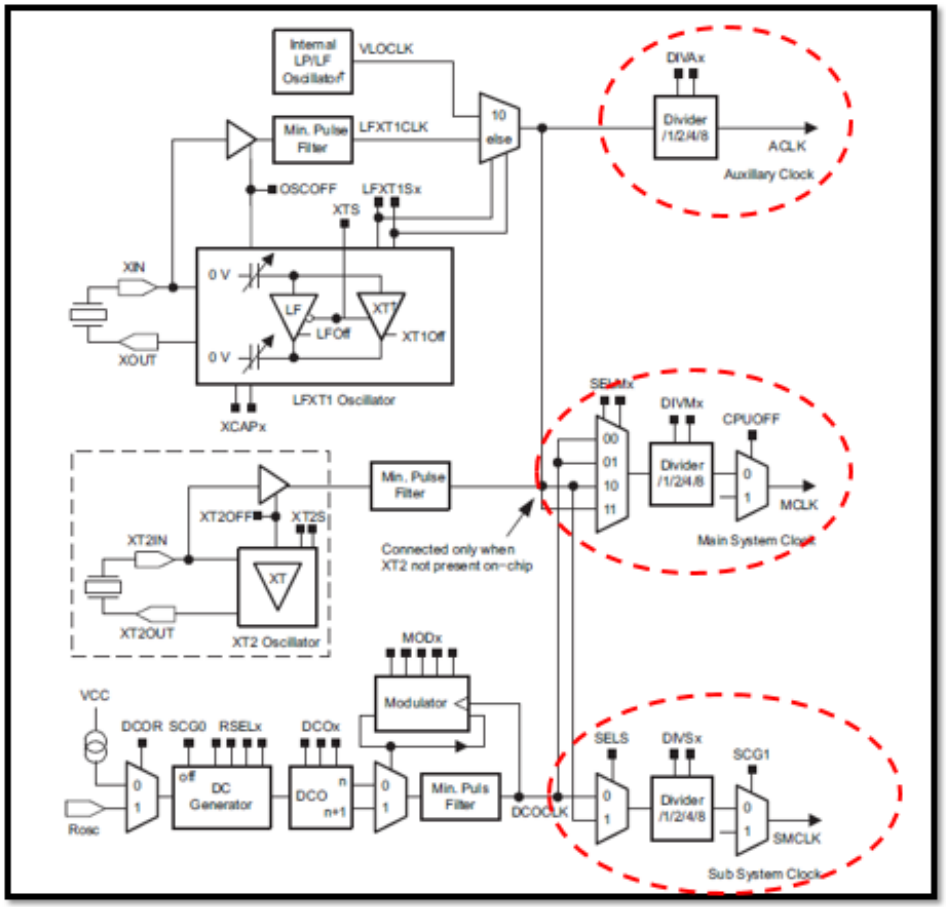
Basic Clock Module+

Clock Signals

–ACLK: Auxiliary Clock. The signal is sourced from LFXT1CLK with a divider of 1, 2, 4, or 8. (The calibration program for the serial link sets the divider to 4, but after the calibration it can be changed to any other values.)

–MCLK: Master Clock. The signal can be sourced from LFXT1CLK, XT2CLK or DCOCLK with a divider of 1, 2, 4, or 8. MCLK is used by the CPU and system.

–SMCLK: Sub-Main Clock. The signal is sourced from either XT2CLK or DCOCLK with a divider of 1, 2, 4, or 8. SMCLK can be used as the clock signal for Timer A and Timer B.



Select Digital I/O Registers

Function Select Registers: (**PxSEL**) and (**PxSEL2**):

PxSEL	PxSEL2	Pin Function
0	0	Selects general purpose I/O function
0	1	Selects the primary peripheral module function
1	0	Reserved (See device-specific data sheet)
1	1	Selects the secondary peripheral module function

Use your lecture notes and the MSP430 Device Datasheet as a reference!

Low-Power Modes Available

- **Active Mode (AM)**: CPU, all clocks, and enabled modules are active (≈230 µA)
- **LPM0**: CPU and MCLK are disabled, SMCLK, ACLK and DCO remain active (≈56 µA)
- **LPM2**: CPU, MCLK, and SMCLK are disabled; only ACLK and DCO remain active (≈22 µA)
- **LPM3**: CPU, MCLK, SMCLK, and DCO are disabled; only ACLK remains active (≈0.5 µA)
- **LPM4**: CPU and all clocks disabled, RAM is retained (≈0.1 µA)

Play with your code to test out the differences between each LPM!

Output Screen