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Low Power Tiered Wake-up Module for Lightweight Embedded Systems using Cross Correlation

Roozbeh Jafari
Department of Electrical Engineering
Univeristy of Texas at Dallas, Richardson, TX 75080–3021
Email: rjafari@utdallas.edu

***Abstract*—A major objective in design of wearable and light-weight embedded systems is reducing the power consumption. This leads to reduction of the battery size and enhances the wearability of the system. In this paper, we propose an ultra low power tiered wake-up architecture with signal processing capability. The signal processing is based on template matching and normalized corss correlation. The template matching at the beginning is performed with low sensitivity (with fewer bits and samples) but at very low power. Initial template matching removes signals that are obviously not of interest. If the signal is likely to be of interest, the sensitivity and the power consumption of the template matching blocks are gradually increased, until the signal of interest is detected with a reasonable confidence. Consequently, a microcontroller is activated for additional processing. The tunable parameters for template matching include the number of samples, the size of template (window size) and the number of bits per sample. The proposed architecture can enable the next generation of ultra low power or even batteryless wearable and implantable computers due to tremendously reducing the power consumption of the signal processing. We estimate that the power consumption of the proposed tiered wake-up circuitry will be three to six orders of magnitude smaller than state-of-the-art low power microcontrollers, depending on the complexity of the template matching. Further, the proposed architecture provides high level of programmability which is lacking in ASIC architectures custom built for applications.**

***Index Terms*—Wearable computers, Body sensor networks, Low power processing.**

I. Introduction

Light-weight wearable computers, also called Body Sensor Network (BSNs) or Body Area Networks (BANs), bring to fruition many opportunities to continuously monitor human body with sensors placed on the body or implanted in the body. These platforms will revolutionize many application domains including health care and wellness. In the past few years, new wearable applications have evolved and proved to be effective. Yet, one of the major obstacles is the size and the weight of the sensor units. Smaller wearable units can enhance comfort and wearability. Batteryless units operating on energy harvesting, or units that require significantly smaller batteries, are not currently possible. The proposed technique aims to significantly reduce the power consumption of wearable units, and specifically the processing architecture.

Wearable sensor units are often composed of sensors, a processing unit (e.g. a microcontroller), a communication unit and a battery. The target application space of this paper is wearable motion sensors that are used to detect human actions such as 'Sit to Stand' or 'Walking'. We propose an architecture, as shown in Fig. 1, equipped with a *tiered wake-up circuitry*, that monitors incoming signals or actions with a coarse to fine grained sensitivity. The tiered wake-up circuitry attempts to detect actions that are not of interest as early as possible while consuming the least amount of energy. If the incoming action is not of interest, the remaining modules remain inactive. If the incoming action is likely to be of interest, the module will turn on the main signal processing unit (e.g. the microcontroller) for further processing. The decision making is done in a sequence of coarse to fine grained operations. At the beginning, the *screening*

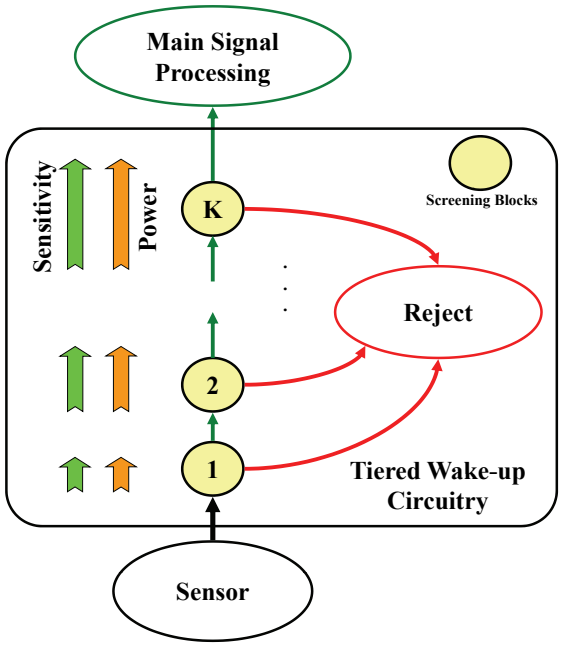

Fig. 1. Tiered Wake-up Circuitry.

or preliminary signal processing may not exhibit high accuracy for classifying the incoming actions, but operates at an ultra low power. The objective is to identify *incoming actions* that are *obvious* rejects. As the module begins to observe incoming actions that are *likely* of interest, more accurate decision making and screening processes are activated. This is done by tuning several parameters on the screening blocks including the time duration of the actions, the number and the location of samples within each action, and the bit resolution of the samples. Collectively, screening blocks can select any combination of these parameters to adjust power vs. sensitivity. The decision making is performed in this fashion because often the incoming action is so dissimilar to the *action of interest* (also called target action) that it can be rejected even with a coarse grained signal processing. The main advantage of this method is the power saving due to removing actions that are not of interest from the signal processing chain as early as possible at the lowest power, deactivating the remaining modules in the signal processing chain.

Applications of health care monitoring have unique properties motivating our proposed technique: *Events or actions of interest* often occur with a low duty cycle (e.g. $< 1\% - 5\%$). That is, the microcontroller does not need to be active all the time. Events are slowly changing and the randomness to the incoming signals, even in cases where the signals are not of interest, is not significant (i.e.

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TABLE I
MINI-SEGMENT OPTIMIZATION

# of Mini Segments	Resolution (bits)	Mini Segment Length (# of samples)	Mini Segments Used	Power (nW)
2	12	150	$\#1 \rightarrow \#2$	6.81
5	12	60	$\#2 \rightarrow \#1$	2.72
10	12	30	$\#3 \rightarrow \#1$	1.36
15	12	20	$\#3 \rightarrow \#5$	0.91
20	12	15	$\#2 \rightarrow \#6$	0.68
25	12	12	$\#2 \rightarrow \#8$	0.54
30	12	10	$\#3 \rightarrow \#9$	0.45

TABLE II
OPTIMIZATION FOR BIT RESOLUTION

Sensitivity (%)	Template Length (# of samples)	Bit Resolutions Used	Power (nW)
50	300	$1 \rightarrow 9$	5.68
60	300	$3 \rightarrow 9$	6.20
70	300	$3 \rightarrow 10$	6.64
80	300	$4 \rightarrow 10$	6.76
90	300	$4 \rightarrow 11$	6.84
95	300	$4 \rightarrow 11$	7.02

events can be represented by templates). These assumptions hold for many wearable applications where the objective is to detect sparse events such as walking, using motion sensors, or cardiac arrest and seizures, using implantable sensors. We utilize these unique properties to propose our novel tiered wake-up architecture. Although in our approach, every effort will be taken to ensure that the tiered wake-up module provides acceptable precision for signal processing, in the events where it generates *false positives*, the sole drawback is the energy consumed to wake up the main signal processing unit for further signal processing. Finally, the events are captured with a low sampling rate (e.g. $\leq 100Hz - 1kHz$) which implies that the processing can also be done at a slow speed, and hence at a very low power.

II. RELATED WORK

Several ultra low power wearable systems, with signal processing capabilities, at the power budget of less than hundreds of μW have been proposed. The proposed systems, however, are either not programmable (except that they may provide a few tunable parameters), or the programmability is handled completely by a microcontroller [1], [2], [3].

Our low power architecture, which aims at less than few hundreds of nW power budget, is different from the previous work for the following reasons: 1) the decision making is tightly integrated with the power and is performed in a sequence of low to high sensitivity, 2) the proposed architecture takes into account specific properties of the signal processing in wearable applications, 3) our screening module is reprogrammable, and multiple signals of interest (or templates) can be loaded and reloaded on-the-fly or off-line onto the architecture.

III. PROPOSED ARCHITECTURE

A. Tiered Wake-up Module

The tiered wake-up module, which is composed of several coarse to fine grained screening classifiers, is responsible for screening sensor readings and activating main processing unit upon arrival of an event (or action) of interest. The screening is implemented by template matching using normalized cross correlation. Normalized cross correlation has proved to be effective for shape based template matching, and can be easily implemented in hardware using simple adders and multipliers.

The tunable parameters for template matching include the time duration of actions considered for cross correlation calculation, the number and the location of samples within each action, and the bit resolution for samples. This allows to adjust the power and the sensitivity of the signal processing in each template matching block.

IV. OPTIMIZATION AND EXPERIMENTAL RESULTS

Our architecture can be optimized for various tunable parameters. The tiered wake-up module is essentially a decision path including a series of low power screening blocks operating with different bit resolutions and number of samples per action, as shown in Fig. 1. The objective of the optimization is to find optimal decision path that minimizes the power while maintaining an acceptable precision and sensitivity. In the following, we present our results for optimizing the bit resolution and the number of samples.

For our preliminary study, we collected data from five participants each wearing a 3-axis accelerometer on their waist. Every participant performed seven actions (e.g. 'sit to stand', 'sit to lie', etc.), 20 times each. 'Sit to stand' was assumed to be the target action. We used this data for template generation and matching. The accelerometer was sampled at $50Hz$. To estimate power consumption of the template matching blocks, they were implemented using Verilog and synthesized using Synopsys with the $45nm$ NanGate Open Cell library. Power measures were further computed with switching activity generated by the real sensor data. The sensor data are often slowly changing, resulting in perhaps small chnages in a few LSBs. This generates smaller number of transitions and minimally affects the swicthing power of the mutipliers and adders.

Our preliminary study shows that only smaller portions of incoming signals are sufficient to detect the target action. For this, we divide each action/template into several mini segments and find the minimum subset of mini segments that can detect the target movement and activate the main signal processing block. We use Integer Linear Programming (ILP) to select the lowest cost decision path and its corresponding mini segments while the required sensitivity of the decision path was enforced as a constraint. Table I shows optimal decision path for various number of mini segments, ranging from 2 to 30. In each case, ILP only selected two screening blocks as demonstrated in the fourth column. The last column shows the power consumption of the decision path, which is clearly six orders of magnitude smaller than state-of-the-art low power microcontrollers operating at mW range. A more detailed description of decision path for the case of 30 mini segments is as follows: The path had only two template matching blocks for mini segments $\#3$ and $\#9$. Out of all incoming actions, 83% were rejected by mini segment $\#3$ resulting in 17% of the movements being passed to the second screening block, processing mini segment $\#9$. The second screening block rejected another 3.7% of the incoming actions leaving only 13.3%, to be passed to the microcontroller. The decision path for all cases in Table I was designed to ensure a sensitivity of $> 95\%$.

In the second set of experiments, we determine the decision path with the lowest power cost while varying the bit resolution and the sensitivity constraints (first column in Table II), using ILP again. As shown in Table II, for example, for the sensitivity of 90%, cross correlation is computed on a 300 sample window at a 4-bit resolution followed by a 10-bit resolution. In all cases, only two template matching blocks are chosen by the ILP. The last column in Table II shows the energy consumption corresponding to the decision path. We note that the first screening block (e.g. 3-bit or 4-bit template matching blocks) is active all the time. However, the second screening block is activated based to the outcome of the previous template matching (if it generates an *accept*). Therefore, the power numbers not only depend on the bit resolution, but also the number of action passed from the first block to the second.

V. Conclusion and Future Work

We proposed an ultra low power signal screening architecture for power saving in light-weight embedded systems. This processing model operates based on a series of coarse to fine grained template matching blocks that can be optimized with several tunable parameters. These blocks activate main processor only upon observing an action of interest, keeping main processor inactive most of the time. Our preliminary results show that the proposed preprocessing module consumes several orders of magnitude less power than typical microcontrollers.

The decision paths determined in this paper are static, obtained using an ILP formulation and are targetted to detect only one movement at a time. In future, we will investigate polynomial time algorithms that determine the decision paths, and investigate dynamic adjustment of the decision paths in the presence of multiple target movements, or variations of a specific target movement (e.g. due to speed, environmental variations). In addition, software and architecture support to accomodate reconfiguration of the decision paths, off-line or on-the-fly, will be investigated. Finally, normalized corss correlation in time domain, although appear to be sufficient for our pilot study, may not well extend to a broader set recognition algorithms. For periodic movements (e.g. walking), frequency domain analysis has proved to be more effective. For movements that exhibit larger speed variations, other approaches such as dynamin time warping [4] or perhaps, performing matching on other feature spaces will be useful.

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