# A Low Power Wake-Up Circuitry Based on Dynamic Time Warping for Body Sensor Networks

Roozbeh Jafari, Reza Lotfian
Embedded Systems and Signal Processing Laboratory
The University of Texas at Dallas
rjafari@utdallas.edu, rxl099220@utdallas.edu

## ABSTRACT
Enhancing the wearability and reducing the form factor often are among the major objectives in design of wearable platforms. Power optimization techniques will significantly reduce the form factor and/or will prolong the time intervals between recharges. In this paper, we propose an ultra low power programmable architecture based on Dynamic Time Warping specifically designed for wearable inertial sensors. The low power architecture performs the signal processing merely as fast as the production rate for the inertial sensors, and further considers the minimum bit resolution and the number of samples that are just enough to detect the movement of interest. Our results show that the power consumption for inertial based monitoring systems can be reduced by at least three orders of magnitude using our proposed architecture compared to the state-of-the-art low power microcontrollers.

## Keywords
Body Sensor Network, Dynamic Time Warping, Tiered Wake-up Circuitry.

## I. INTRODUCTION
Recently, light weight wireless Body Sensor Networks (BSN) has attracted considerable attention from researchers in several application domains including health-care and well-being. BSNs can continuously monitor human body, collect physiological data, perform signal processing, and activate actuators in real-time. Prior research has investigated applications in gait analysis [1], sports medicine [2], fall detection and geriatric care [3]. Wearability, small form factor and ease of use in BSNs are probably the most significant factors promoting the compliance and the continuous use of BSNs. Battery size is the dominant factor affecting the wearability. Power reduction techniques can improve the battery life and reduce the battery size. System level power optimization techniques that consider all subsystems in BSN platforms including sensing, processing, and communication subsystems have been an attractive solution due to the tight integration of BSN subsystems. Among all subsystems, the wireless communication module is often the most power hungry subsystem. Transmitting raw sensor data continuously through the radio link shortens battery life. Hence, data reduction techniques, and local signal processing can enhance the power lifetime of the system.

A kind of body sensor networks that has attracted much interest is inertial wearable systems. Recent advances in MicroElectroMechanical Systems (MEMS) introduced low power and small size accelerometers and gyroscopes which can be attached to the human body and monitor daily activities without much noticeable discomfort. The inertial based BSN nodes can detect various movements such as walking, lying down, sit to stand, among many others. If readings from more than one wearable node are required to detect a movement, a base station can combine readings and perform the data fusion.

Local signal processing involves observing all sensor readings, specifically, all samples from the sensors. Typically, inertial based BSN platforms have sampling frequency of 20-100 Hz and with resolution of 10-12 bits per sample. A movement with duration of 2 seconds includes roughly 40-200 samples (at 10-12 bits per sample). One straight-forward signal processing approach is to consider all samples. However, in many instances, an incoming movement is considerably dissimilar to the movement of interest (or target movement) and it can be rejected as a non-target movement even with a smaller number of samples at a lower bit resolution. We use the intuition behind this approach to design our low power architecture, which we call the *Granular Decision Making Module*. Granular decision making module initially performs the signal processing with lower sensitivity (i.e. observes smaller number of samples and bit resolution). If the incoming signal appears not to be of interest, it will be removed from the signal processing chain immediately and the consecutive signal processing modules remains inactive. Otherwise, modules with higher sensitivity (and power) are activated to further examine if the incoming signal is of interest. Finally, the incoming signal, that appears to be of interest, is passed to a microcontroller in case extra parameters need to be extracted.

Temple matching is the core of granular decision making module. Template matching can be realized with various techniques including cross correlation [4] and Dynamic Time Warping (DTW) [5]. Human movements can be performed with various speeds. Therefore, a speed insensitive template matching module would be desirable. Dynamic time warping techniques are designed to take into account speed variations; hence, we adopt DTW template matching approach in our proposed architecture.

## II. RELATED WORKS
Several power optimization techniques have been suggested for BSNs to enhance the wearablity and the battery life of the system. Zappi et al. [6] suggested techniques for dynamically selecting and activating motion sensors. Authors in [7] proposed a wireless power transmission based on inductive coupling that harvests energy with an adaptive threshold rectifier to detect irregular heart activities in an eight day period. In another work, a vibration based energy harvesting system is suggested that operates with a power budget of 36.79μW [8]

Dynamic Time Warping (DTW) is widely used in speech-recognition [9][10], for online signature verification [11] and for fall detection in the elderly [12]. However, none of the prior

978-0-7695-4431-1/11 $26.00 © 2011 IEEE
DOI 10.1109/BSN.2011.43

works has investigated DTW in line with power optimization. Special purpose architectures are proposed for the implementation of DTW. In [13], a systolic array architecture was proposed for an accelerated DTW operator. Cheng et al. proposed a VLSI architecture for handwriting recognition based on DTW [14]. Wang et al. designed a chip for portable speech recognition for persons with hearing disabilities [15]. In this work, a parallel lattice design was proposed to improve the performance of the DTW architecture. The main objective of all the previous works has been enhancing the speed of DTW and reducing its complexity. None has explored the notion of the granular signal processing, decision making and the use of DTW with tunable parameters (e.g. bit resolution and the number of samples).

# III. ARCHITECTURE FOR WEARABLE COMPUTERS

This section describes an overall architecture of a wearable unit with the proposed granular decision making module (as shown in Figure 1). This module allows for low power signal pre-conditioning prior to activating more power-hungry processing units. While this platform can be used for a variety of applications, we present the proposed architecture in the context of physical movement monitoring where human actions are analyzed by a wearable unit for diagnosis, treatment, or providing clinical decision supports.

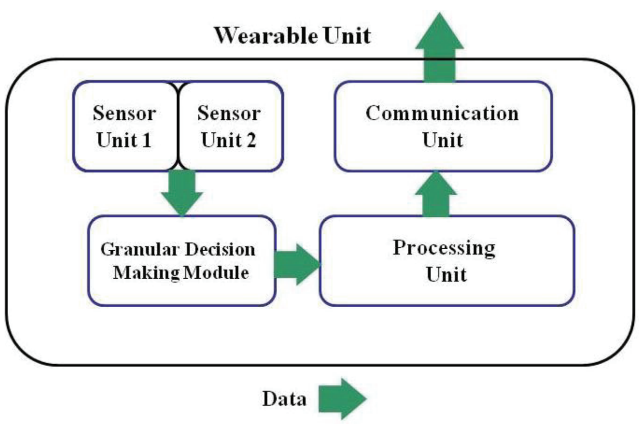


**Figure. 1. A wearable node with sensing, granular decision making, processing, and communication modules.**

## A. Motivation

Many physical movement monitoring applications deal with a small subset of human movements. For example, gait analysis only is concerned with walking, fall detection with falls, Parkinson's disease monitoring with certain movements such as tremor and sleep apnea with restless leg movements [16]. These target movements may occur infrequently. Considerable energy is wasted processing movements that are not of interest. Efficiently rejecting non-target movements with a pre-conditioning module could lead to a significant increase in battery lifetime.

## B. Sensor Unit

A typical wearable unit consists of sensing units that capture physiological information from the user. Depending on the application, a variety of sensors can be used. For example, accelerometers, gyroscopes, and magnetometers are typically used for monitoring and analysis of human movements.

## C. Granular Decision Making Module

A granular decision making module is composed of low power template matching blocks with several tunable parameters that can adjust the sensitivity (and the power) of the signal processing. We design our template matching blocks based on the concept of Dynamic Time Warping, which will be illustrated in Section E.

## D. Processing Unit

The main goal of signal processing is to extract useful information from sensor data. Examples for the objectives of signal processing include "Is the subject running?" or "What is the stride length when the subject is walking?". Microcontrollers can be ideal to extract this information. Their programmability enables the application developers to literally develop any signal processing algorithms. Microcontrollers, or the main signal processing units, provide a *fully* software programmable environment for development of signal processing techniques.

Signal processing algorithms are designed to accommodate the objectives of the application. For example, the goal of action recognition [17, 18, 19] is to classify human movements to a set of predefined actions such as 'sit to stand', 'walking', 'sit to lie', and 'kneeling'. Typically, this is performed using pattern recognition techniques [20] and requires several steps including filtering, feature extraction, and classification. The sampled data are filtered to improve signal to noise ratio. A set of statistical features extracted from individual segments. At the end, classification techniques (e.g. $k$-Nearest Neighbor [20]) are utilized to identify the action performed by the subject wearing the system, and possibly extract other relevant information (e.g. the duration of sit to stand).

In this paper we focus on designing an ultra low power wake-up granular decision making module which monitors incoming sensor data and sends a wake-up signal to the microcontroller or the main processing unit, in case a signal of interest is detected.

# IV. ARCHITECTURE FOR TEMPLATE MATCHING BLOCKS

## E. Preliminaries

### *Dynamic Time Warping*

Template matching techniques are effective for movement monitoring applications. This is done by matching continuous incoming signals received from inertial sensors against a pre-defined waveform (or template) that represents a movement of interest. An effective template matching block needs to function properly despite speed and cross subject variations in movements.

DTW techniques are effective for signals with speed variations. They use a dynamic programming approach to align an unknown sequence with a specific template subject to minimizing a distance measure. The details of the distance measure are illustrated in Section IV.F.

Suppose we have two sequences, $T$ and $S$, of length $m$ and $n$, developed along the two imaginary axes ($i$-axis and $j$-axis), respectively, where

$$T = t_1, t_2, \dots, t_i, \dots, t_m \tag{1}$$

$$S = s_1, s_2, \dots, s_j, \dots, s_n \tag{2}$$

A warping path is a sequence of points $w = (i, j)$

$$W = w_1, w_2, \dots, w_k, \dots, w_p, \tag{3}$$

where

$$w_k = (i_k, j_k) \tag{4}$$

To align two sequences with DTW, we construct a $m \times n$ matrix where the element $(i,j)$ is the distance $d(t_i, s_j)$ between two points $t_i$ and $s_j$. A warping path $W$, aligns the elements of $S$ and $T$ such that distance between vectors S and T are minimized

In general, the following constraints must hold for the warping path [5]:

1. Monotonicity: The points in the path must be monotonically spaced in time, $i_{k-1} \le i_k$ and $j_{k-1} \le j_k$
2. Continuity: The allowable transitions are limited to adjacent points, $i_k - i_{k-1} \le 1$ and $j_k - j_{k-1} \le 1$
3. Boundary Conditions : Confine the start and finish point of the warping path

In the most restricted variant of boundary conditions, the path requires to start and finish diagonally on the opposite corner elements of the matrix i.e. $w_1 = (1,1)$ and $w_K = (m,n)$. Even in the above case, there exists exponential number of warping paths. However, we are only interested in the path with the minimum cost, defined as:

$$DTW(S,T) = \min_{W} \left\{ \sum_{k=1}^{p} d\big(w(k)\big) \right\} \tag{5}$$

The optimal path can be found using dynamic programming approach. The cumulative distance, $\gamma(i,j)$, defined as the shortest possible path to point $(i,j)$. Due to continuity condition, we have:

$$\gamma(i,j) = d\big(t_i, s_j\big) + min \begin{cases} \gamma(i-1,j) \\ \gamma(i,j-1) \\ \gamma(i-1,j-1) \end{cases} \tag{6}$$

Assuming that $\gamma(1,1) = d(t_1, s_1)$, the cumulative distances calculated according to the above equation. Figure 2 shows legal transitions according to continuity condition, as also highlighted in Equation 6.

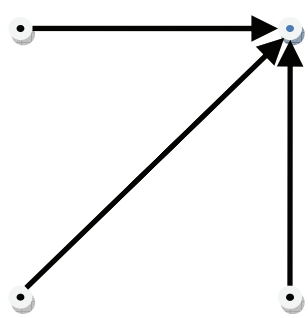

**Figure. 2. Legal transitions**

### *Dynamic Time Warping for continuous streams of data*

In wearable computers, continuous streams of samples are received from sensor. Therefore, sequence of $S$ is semi-infinite time series and boundaries are unknown. Therefore, start point could be any point in the sequence. It is required to update the search for the shortest path for every sample in the sequence [21]. Thus, boundary conditions are modified to be $w_1 = (1, j_1)$ and $w_2 = (m, j_2)$. The only modification needed for this boundary condition is defined in Equation 7.

$$\gamma(1,j) = d\big(t_1, s_j\big) \tag{7}$$

## F. Architecture Design

We utilize 3-axis accelerometers in our wearable platforms. Hence, a three dimensional stream of data that are received from the accelerometers are forwarded to the DTW modules. We use Euclidean distance for $d\big(w(k)\big)$. Since calculation of square root in Euclidian distance is relatively complex in hardware, we also use square of the Euclidian distance in a separate analysis. We first calculate $|x_i - \hat{x}_j|$, $|y_i - \hat{y}_j|$ and $|z_i - \hat{z}_j|$ and then calculate the sum of their squares. If sensor readings are represented with low bit resolutions, these calculations can be modeled using look-up tables. We implemented the dynamic programming algorithm for DTW as shown in Figure 3.

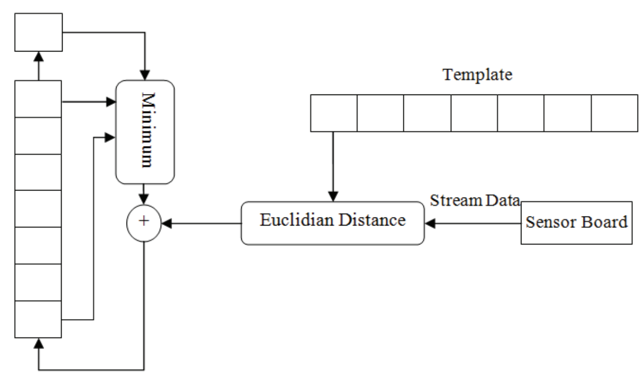


**Figure. 3. DTW architecture for streaming data**

For every new sensor reading, we calculate the distance to the template values. After determining all $d\big(t_i, s_j\big)$, we find $\gamma(i,j)$ as illustrated in Equation 6. We only save the last *m* distances in a shift register for the next sensor reading and calculations for $\gamma(i, j+1)$. When all cumulative distances are calculated, the total warping cost is determined. If the wrapping cost is smaller than a threshold, the microcontroller is activated and the original sensor readings, vector *S*, is passed to the microcontroller.

# V. EXPERIMENTAL RESULTS

We conducted several experiments to establish the effectiveness of our proposed approach. Five subjects were asked to perform movements listed in Table 1. Each movement was performed 10 times. All subjects wore a sensor node on to the waist. The node was programmed to sample three data streams (X, Y and Z axes of an accelerometer) at 72 Hz. The data were collected and imported to MATLAB for analyses related to the DTW.

Reducing bit resolution and sampling rate can reduce the computational load (and the power consumption) of the DTW operation. In several instances, we reduced the sampling frequency and the bit resolution of the incoming sensor readings. However, the original signal with higher bit resolution and sampling frequency is stored, in the case the incoming signal appears to be of interest, the final signal processing using the microcontroller can be performed on the original signal.

**Table 1. List of movements**

| No. | Movement | No. | Movement |
|---|---|---|---|
| 1 | Sit to stand | 6 | Look behind |
| 2 | Sit to lie | 7 | Step forward |
| 3 | Bend to grasp | 8 | Step leftward |
| 4 | Kneel | 9 | Grasp from shelf |
| 5 | Turn right | 10 | Jump up |

DTW requires a template for the target movement. To select the best template, the distances between all trials of the target movement are considered, and the trial with minimum average distance to all is selected as the template:

$$Template = \{T_k | k = \underset{i=\{trials\}}{\operatorname{argmin}} \sum_{j=\{trials\}} DTW(T_i, T_j)\} \qquad (8)$$

For DTW to discriminate between target and non-target actions, we defined a safe margin metric as:

$$SafeMargin_{f,b} = \frac{min(nontarget_{f,b}) - max\,(target_{f,b})}{min(nontarget_{f,b}) + max\,(target_{f,b})} \qquad (9)$$

where $f$ is the frequency of sampling, $b$ is the bit resolution, $\min(\text{nontarget}_{f,b})$ is the minimum DTW distance between the template and all trials of non-target movements and $\max(\text{target}_{f,b})$ is the maximum DTW distance between the template and all trials of the target movement. Safe margin can also be viewed as the discrimination boundary between target and non-target movements. Hence, large safe margins correspond to more effective classifiers.

Since the distance measure depends on the sampling frequency and the bit resolution, safe margin is normalized to enable fair comparison for various bit resolutions and sampling frequencies.

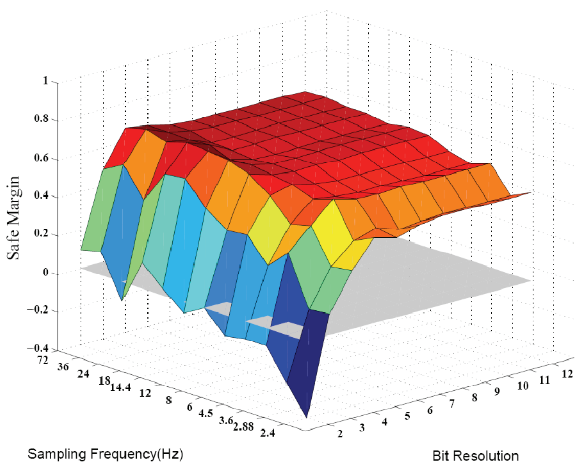


**Figure. 4. Relative DTW margin between target and non-target movements**

In the first set of experiments, we selected 'sit to stand' as the target movement. Figure. 4 shows the normalized safe margins for various sampling rates and bit resolutions. For the majority of configurations, the safe margins appear to be positive which indicates all target movements can be identified correctly. The safe margins begin to drop below zero as the bit resolution and sampling frequency are reduced below 3 bits and 3 Hz, respectively. A negative safe margin indicates that a number of target movements may not be identified properly.

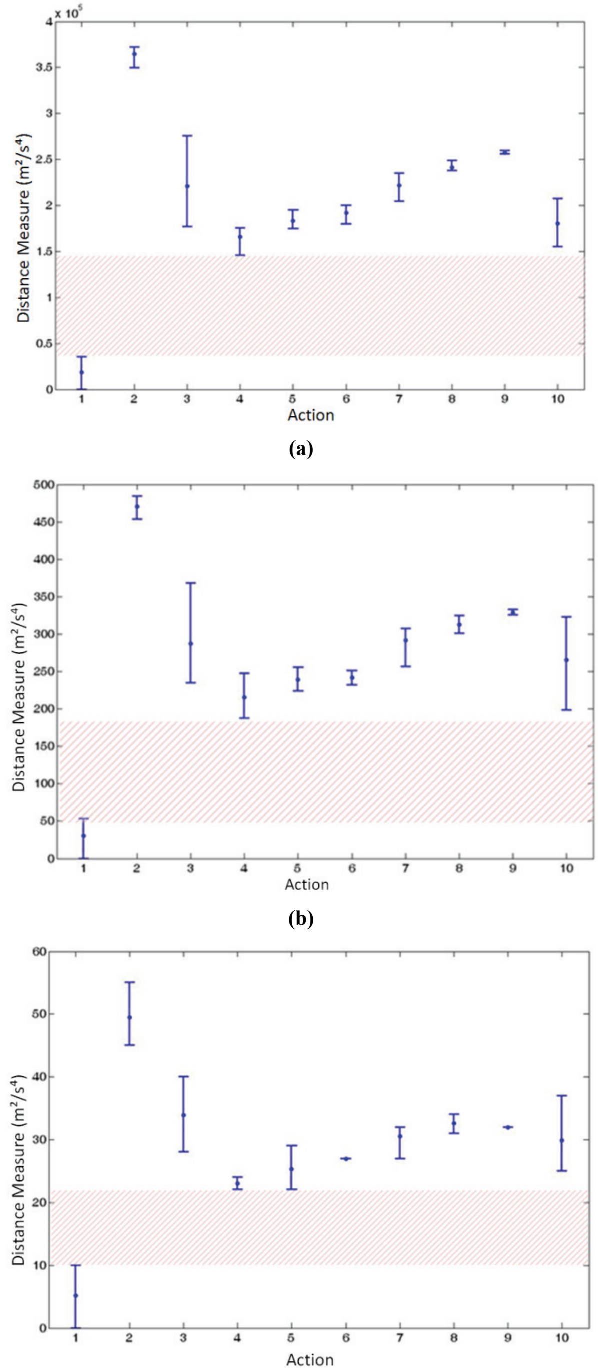


**Figure. 5. Distance measure for movements in Table 1 a) 72 Hz sampling rate and 12 bit resolution. b) 12 Hz sampling rate and 6 bit c) 3 Hz sampling rate and 4 bit**

Figure 5(a) shows the range of DTW distance measures for various movements with $f = 72\,Hz$, $m$ = 167 (number of samples) and $b = 12\,bits$. DTW distance measures for $f =$

$12\,Hz$, $m = 33$ and $b = 6\,bits$ and $f = 3Hz$, $m = 8$, and $b = 4\,bits$ are also illustrated in Figure 5(b) and Figure 5(c), respectively. In all figures, movement (or action) one is the target movement. The area shaded in pink illustrates the safe margin.

In the second sets of experiments, we chose "sit to lie" as the target movement and verified that sampling frequency and the bit resolution can be reduced up to 3 Hz and 2 bits while the safe margin remains positive.

Table 2 shows the safe margins for experiments 1 and 2. Since all safe margin values are positive, DTW can distinguish between movements with accuracy of 100%.

**Table 2. Safe margins for experiments 1 & 2 (target movements: "sit to stand" and "sit to lie")**

| | Sit to stand | Sit to lie |
|---|---|---|
| $f = 72\,Hz$ $k = 12bits$ | 0.602 | 0.686 |
| $f = 12\,Hz$ $k = 6bits$ | 0.594 | 0.685 |
| $f = 3\,Hz$ $k = 4bits$ | 0.375 | 0.385 |

## G. Complexity

In this section, we illustrate the arithmetic complexity of our proposed DTW hardware architecture. With sampling frequency of *f*, bit resolution of *b* and template size of *m* samples, the number of multiplications and additions per second, as well as the size of shift registers are summarized in Table 3.

**Table 3. Number of arithmetic operations and size of shift registers**

| | |
|---|---|
| Multiplication | $3fm/second$ |
| Addition | $8fm/second$ |
| Shift register size | $b*(m+1)\ bits$ |

For example, for $f = 3\,Hz$, $b = 4$ and $m = 8$, the complexity of the design is illustrated in Table 4.

**Table 4. Number of arithmetic operations and size of shift registers for *f* = 3 Hz, *b* = 4 bits & *m* = 8 samples**

| | |
|---|---|
| Multiplication | $84\ /second$ |
| Addition | 244 /second |
| Shift register size | 72 bits |

## H. Hardware Implementation

Our proposed architecture for DTW was implemented in Verilog. The design was synthesized with Synopsys using the 65nm process technology. Power analysis was performed with DesignVision on various design instances including ($f = 72\,Hz\ m = 167, k = 12bits$), ($f = 12\,Hz, m = 33, k = 6bits$) and ($f = 3\,Hz, m = 8, k = 4bits$). The area, dynamic, leakage and total power numbers for various DTW instances are illustrated in Table 5.

**Table 5. Performance summary**

| | $f = 72\,Hz$, $b = 12bits$ | $f = 12\,Hz$, $b = 6bits$ | $f = 3\,Hz$, $b = 4bits$ |
|---|---|---|---|
| Total Area | 51549 μm² | 9665 μm² | 2116 μm² |
| **Dynamic power** | **1.9 nW** | **304 pW** | **57 pW** |
| Leakage Power | 193 μW | 37 μW | 9 μW |
| Total Power | 193 μW | 37 μW | 9 μW |

In our proposed architecture, the operational frequency of the circuit is very low (e.g. around 50 Hz), hence, we observed that the leakage power dominates the total power. We used an available library for 65 nm process technology due lack of access to other suitable libraries. However, we intend to acquire libraries with larger transistors that have reduced leakage power [22].

Comparing these results to template matching algorithms implemented in microcontrollers clarifies that our proposed architecture has tremendous power advantage over a typical microcontroller (e.g. power consumption of MSP430 is 3 mW in active mode). In particular, considering f = 3 Hz and b = 4 bits configuration, a roughly three orders of magnitude power reduction was achieved. Assume a wearable node that includes a 1.25 mW 3-axis accelerometer, a 3 mW microcontroller (e.g. MSP430), and a 9 μW wake-up circuitry that detects sit to stand, with frequency of occurrence of 6 per hour with maximum duration of 5 seconds per movement. With this wearable node, the average power consumption measures at (1.25mW + 9 μW) + (3 mW * 6 * 5 / 3600) = 1.28 mW. The overall power consumption here is mainly dominated by the power consumption of the sensor.

# VI. CONCLUSION AND FUTURE WORK

In this paper, we presented a granular decision making architecture based on dynamic time warping template matching techniques. This architecture screens sensor readings while consuming very low amount of energy. In case, the sensor readings exhibit the signal of interest (or so called the target movement in this paper), the architecture activates the microcontroller. The basic block of the granular decision making module based on dynamic time warping was designed, implemented using Verilog and verified. The measures on power consumption and the signal processing performance for the DTW were presented.

In terms of the future work, the architecture for the granular decision making module will be fully implemented, with the capability to adjust tunable parameters on the fly (i.e. sampling frequency and bit resolution). Further, larger transistors will be used in hardware implementation to reduce the leakage power. Finally, the proposed architecture will be validated with more extensive movement data sets.

# VII. REFERENCES


[1] E. Jovanov, A. Milenkovic, C. Otto, and P. De Groen, "A wireless body area network of intelligent motion sensors for computer assisted physical rehabilitation," *Journal of NeuroEngineering and Rehabilitation*, vol. 2, pp. –, 2005.

[2] J. Pansiot, B. Lo, and G.-Z. Yang, "Swimming stroke kinematic analysis with bsn," in *2010 International Conference on Body Sensor Networks, BSN 2010*, 2010, pp. 153–158.

[3] J. Chen, K. Kwong, D. Chang, J. Luk, and R. Bajcsy, "Wearable sensors for reliable fall detection," in *Annual International Conference of the IEEE Engineering in Medicine and Biology - Proceedings*, vol. 7 VOLS, 2005, pp. 3551–3554.

[4] O. Liseth, H. Hjortland, and T. Lande, "Power efficient cross-correlation beat detection in electrocardiogram analysis using bitstreams," in *Biomedical Circuits and Systems Conference, 2009. BioCAS 2009. IEEE DOI - 10.1109/BIOCAS.2009.5372041*, 2009, pp. 237–240.

[5] L. Rabiner and B. Juang, *Fundamentals of Speech Recognition*, pp. –, 1993.

[6] P. Zappi, C. Lombriser, T. Stiefmeier, E. Farella, D. Roggen, L. Benini, and G. Troster, "Activity recognition from on-body sensors: Accuracy-power trade-off by dynamic sensor selection," pp. 17–33, 2008.

[7] J. Yoo, L. Yan, S. Lee, Y. Kim, and H.-J. Yoo, "A 5.2 mW self-configured wearable body sensor network controller and a 12 μw wirelessly powered sensor for a continuous health monitoring system," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 1, pp. 178–188, 2010.

[8] L. Chao, C.-Y. Tsui, and W.-H. Ki, "A batteryless vibration-based energy harvesting system for ultra low power ubiquitous applications," in *Proceedings - IEEE International Symposium on Circuits and Systems*, 2007, pp. 1349–1352.

[9] G. Quenot, J.-L. Gauvain, J.-J. Gangolf, and J. Mariani, "A dynamic time warp vlsi processors for continuous speech recognition," in *Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP '86. DOI - 10.1109/ICASSP.1986.1168945*, vol. 11, 1986, pp. 1549–1552.

[10] R. Owen, "A vlsi dynamic time warp processor for connected and isolated word speech recognition," in *Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP '85. DOI - 10.1109/ICASSP.1985.1168159*, vol. 10, 1985, pp. 985–988.

[11] R. Martens and L. Claesen, "On-line signature verification by dynamic time-warping," in *Pattern Recognition, 1996., Proceedings of the 13th International Conference on DOI - 10.1109/ICPR.1996.546791*, vol. 3, 1996, pp. 38–42 vol.3.

[12] S. Paiyarom, P. Tungamchit, R. Keinprasit, and P. Kayasith, "Activity monitoring system using dynamic time warping for the elderly and disabled people," in *Computer, Control and Communication, 2009. IC4 2009. 2nd International Conference on DOI - 10.1109/IC4.2009.4909158*, 2009, pp. 1–4.

[13] V. Sundaresan, S. Nichani, N. Ranganathan, and R. Sankar, "A vlsi hardware accelerator for dynamic time warping," in *Pattern Recognition, 1992. Vol. IV. Conference D: Architectures for Vision and Pattern Recognition, Proceedings., 11th IAPR International Conference on DOI - 10.1109/ICPR.1992.202121*, 1992, pp. 27–30.

[14] H.-D. Cheng and K.-S. Fu, "Vlsi architecture for dynamic time-warp recognition of handwritten symbols," *Acoustics, Speech and Signal Processing, IEEE Transactions on DOI - 10.1109/TASSP.1986.1164836*, vol. 34, no. 3, pp. 603–613, 1986.

[15] J.-F. Wang, J.-C. Wang, H.-C. Chen, T.-L. Chen, C.-C. Chang, and M.-C. Shih, "Chip design of portable speech memopad suitable for persons with visual disabilities," *Speech and Audio Processing, IEEE Transactions on DOI - 10.1109/TSA.2002.805645*, vol. 10, no. 8, pp. 644–658, 2002.

[16] M. Ohayon and T. Roth, "Prevalence of restless legs syndrome and periodic limb movement disorder in the general population," *Journal of Psychosomatic Research*, vol. 53, no. 1, pp. 547–554, 2002.

[17] H. Ghasemzadeh, V. Loseu, and R. Jafari, "Structural action recognition in body sensor networks: Distributed classification based on string matching," *IEEE Transactions on Information Technology in Biomedicine*, vol. 14, no. 2, pp. 425–435, 2010.

[18] H. Ghasemzadeh, E. Guenterberg, and R. Jafari, "Energy-efficient information-driven coverage for physical movement monitoring in body sensor networks," *IEEE Journal on Selected Areas in Communications*, vol. 27, no. 1, pp. 58–69, 2009.

[19] H. Ghasemzadeh, J. Barnes, E. Guenterberg, and R. Jafari, "A phonological expression for physical movement monitoring in body sensor networks," in *2008 5th IEEE International Conference on Mobile Ad-Hoc and Sensor Systems, MASS 2008*, 2008, pp. 58–68.

[20] R. Duda, P. Hart, and D. Stork, "Pattern classification," *John Wiley and sons Inc., New York, 2001*, pp. –, 2010.

[21] Y. Sakurai, C. Faloutsos, and M. Yamamuro, "Stream monitoring under the time warping distance," in *Proceedings - International Conference on Data Engineering*, 2007, pp. 1046–1055.

[22] N. Kim, T. Austin, D. Baauw, T. Mudge, K. Flautner, J. Hu, M. Irwin, M. Kandemir, and V. Narayanan, "Leakage current: Moore's law meets static power," *Computer DOI - 10.1109/MC.2003.1250885*, vol. 36, no. 12, pp. 68–75, 2003.